Fully-Depleted, Back-Illuminated Charge-Coupled Devices Fabricated on High-Resistivity Silicon

Stephen E. Holland, Donald E. Groom, Nick P. Palaio, Richard J. Stover, Mingzhi Wei

Abstract— **Charge-coupled devices (CCD's) have been fabricated on high-resistivity silicon. The resistivity, on the order of 10,000 Ω-cm, allows for depletion depths of several hundred microns. Fully-depleted, back-illuminated operation is achieved by the application of a bias voltage to a ohmic contact on the wafer back side consisting of a thin in-situ doped polycrystalline silicon layer capped by indium tin oxide and silicon dioxide. This thin contact allows for good short wavelength response, while the relatively large depleted thickness results in good near-infrared response.**

Keywords— **Charge-coupled device, back illuminated, fully depleted, high-resistivity silicon.**

I. Introduction

THE large focal planes at astronomical telescopes require high quantum efficiency (QE), large format charge-coupled device (CCD) detectors. In order to achieve high QE, the standard scientific CCD is thinned and back illuminated [1]. Thinning is required because the relatively low resistivity silicon used to fabricate scientific CCD's limits the depth of the depletion region. In order to minimize field-free regions with resulting degradation in spatial resolution, the typical scientific CCD is thinned to about 20 μm. This process degrades red response and results in fringing in the near infrared where the absorption depth of the light becomes comparable to the CCD thickness.

Extended red response is extremely important to the Supernovae Cosmology Project at Lawrence Berkeley National Laboratory (LBNL) due to the use of distant, high redshift supernovae for the determination of cosmological parameters [2]. Detection and follow-up spectroscopy of high redshift objects would greatly benefit from CCD's with improved near-infrared response.

We have reported results on a small prototype CCD with high QE extended to 1000 nm [3], [4]. In this work the physical operating principles and technology of this CCD are described along with results on large-format sensors.

II. Background

Figure 1 shows a cross-section of the CCD considered in this work. A conventional three-phase, triple polysilicon gate CCD [5] with buried channel is fabricated on a high-resistivity n-type substrate. A substrate bias is applied to fully deplete the substrate, which is typically 200–300 μm thick. The CCD's described in this work are fabricated on 10,000–12,000 Ω-cm material, corresponding to a donor

S. Holland is with the Lawrence Berkeley National Laboratory, Berkeley, California, USA. E-mail: seholland@lbl.gov .

D. Groom and N. Palaio are with the Lawrence Berkeley National Laboratory, Berkeley, California, USA.

R. Stover and M. Wei are with the University of California Observatories, Santa Cruz, CA.

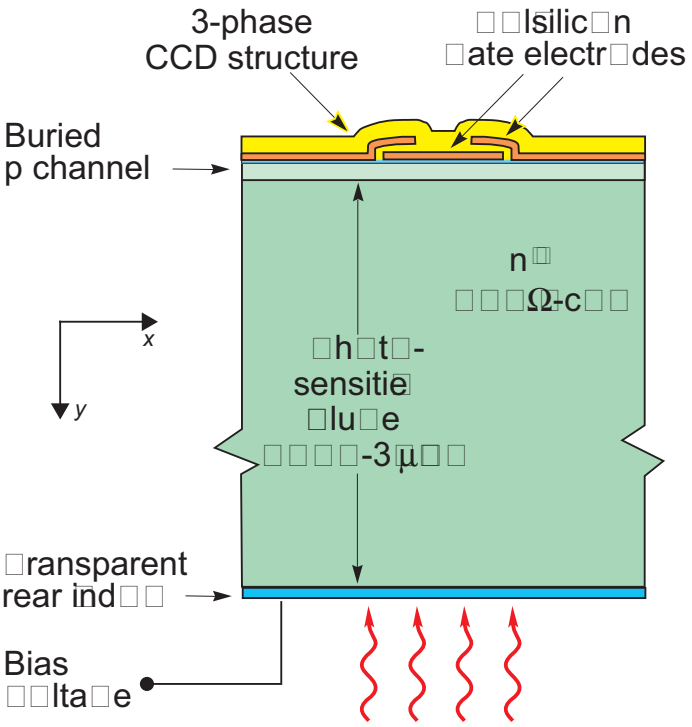


Fig. 1. Cross-sectional diagram of the CCD described in this work.

density N_D of approximately 3.6–4.3 $\times$ 10^{11} cm^{-3}. This high resistivity starting material allows for fully depleted operation at reasonable voltages. The typical operating temperature for the astronomy applications is $-$ 120°C to $-$ 150°C, and enhanced QE is realized with back illumination.

The CCD described here is p-channel. The choice of p-channel over the more conventional n-channel was due to previous work with charged-particle p-i-n detectors fabricated on high-resistivity n-type silicon, where in our experience it was more straightforward to achieve low dark current silicon via backside gettering techniques [6]. The degraded readout speed resulting from lower hole mobility in a p-channel CCD is not a concern for the astronomy application, where readout is slow to minimize read noise (typically 20–50 kpixels/sec [1]).

Previous n-channel "deep-depletion CCD's" [7], [8], [9], [10], [11] have 40–80 μm thick depletion regions, due to the use of more highly doped starting silicon and the lack of a backside bias voltage. Early work on CCD's fabricated on high-resistivity n-type silicon was reported although problems with high dark current were noted [12], [13]. In the prior work cited the interest was in extended x-ray re-

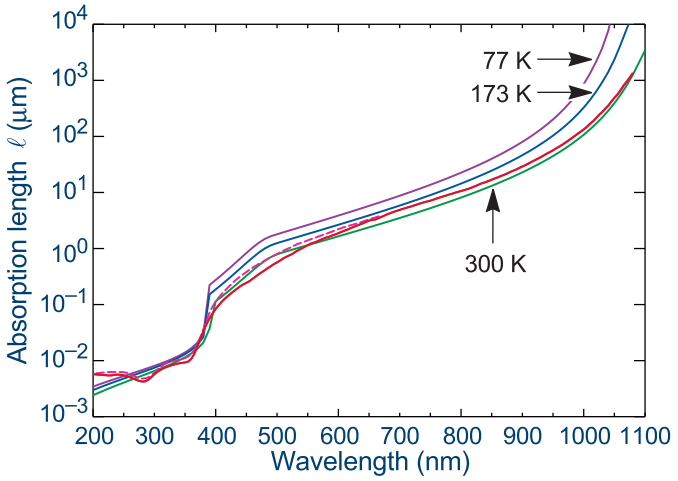


Fig. 2. Absorption length versus wavelength for silicon. Data and calculations are taken from Reference [14]. Additional room temperature data is taken from Reference [1].

sponse. As noted earlier our interest in a thick CCD is motivated by improved near-infrared response. Figure 2 shows calculated absorption length in silicon as a function of wavelength [14]. Absorption length is defined here as the reciprocal of absorption coefficient α defined in terms of attenuation of incident light intensity I_0 with depth y, *i.e.* $I(y) = I_0 e^{-\alpha y}$.

Given that silicon is an indirect-gap semiconductor, two regions are of interest. For photon energies above the direct bandgap energy of 2.5 eV, corresponding to a wavelength of approximately 500 nm, light absorption is highly efficient and the absorption coefficient is determined by available conduction band states [15], [16]. Hence the absorption coefficient for direct transitions α_d varies as the square root of energy as per the energy dependence of the conduction band density of states, *i.e.*

$$\alpha_d = A\sqrt{h\nu - E_{g,\mathrm{direct}}(T)} \tag{1}$$

The temperature dependence is due to the band gap term $E_{g,\mathrm{direct}}(T)$ and is relatively weak in the direct gap regime. A is a constant, $h\nu$ is the photon energy, and T is the absolute temperature.

Below photon energies of 2.5 eV, phonons are required for momentum conservation and the absorption process becomes less efficient and more sensitive to temperature due to the phonon statistics. In the indirect absorption regime the absorption coefficient goes as [15], [16]

$$\alpha_i = \frac{B(h\nu - E_{g,\mathrm{indirect}} + E_p)^2}{\exp(E_p/kT) - 1} + \frac{B(h\nu - E_{g,\mathrm{indirect}} - E_p)^2}{1 - \exp(-E_p/kT)} \tag{2}$$

where the terms are due to phonon absorption and emission, respectively. k is Boltzmann's constant, E_p is the phonon energy, and B is a constant. Eq. 2 is valid for photon energies greater than $E_{g,\mathrm{indirect}} + E_p$ while only the phonon absorption term contributes to the absorption coefficient for photon energies of $E_{g,\mathrm{indirect}} \pm E_p$.

The net result is an absorption length that increases with wavelength as shown in Figure 2. At photon energies comparable to the indirect bandgap the absorption length can be more than 100 μm, requiring thick CCD's to achieve improved near-infrared QE.

Another advantage of a thick CCD is that the CCD clock levels can be set to optimize performance parameters such as charge transfer efficiency and well depth while the substrate bias is used to achieve full depletion. A depletion-approximation solution to the Poisson equation for a thick CCD with applied substrate bias is given in Appendix A. The potential V_J at the buried-channel/substrate junction is approximately

$$V_J \approx V_G - V_{FB} - \frac{qN_A}{2\epsilon_{\mathrm{Si}}} {y_J}^2 \left(1 + \frac{2\epsilon_{\mathrm{Si}} d}{\epsilon_{\mathrm{SiO_2}} y_J}\right) \tag{3}$$

which is independent of the substrate bias voltage V_{sub}. V_G is the applied gate voltage, V_{FB} is the flat-band voltage, q is the electron charge, N_A is the doping density in the p channel of depth y_J, d is the gate insulator thickness, and ϵ_{Si} and $\epsilon_{\mathrm{SiO_2}}$ are the permittivities of silicon and silicon dioxide, respectively.

This approximation is valid for $y_N \gg y_J + (\epsilon_{\mathrm{Si}}/\epsilon_{\mathrm{SiO_2}})\, d$, where y_N is the thickness of the fully-depleted, n-type region (see Figure 15 in Appendix A). This can be rewritten as $C_{DEPL} \ll C_S$ where $C_{DEPL} = \epsilon_{\mathrm{Si}}/y_N$ is the capacitance of the fully depleted n region and C_S is the capacitance of the series combination of the channel and gate insulator capacitors ($\epsilon_{\mathrm{Si}}/y_J$ and $\epsilon_{\mathrm{SiO_2}}/d$, respectively). Hence for a thick depletion region the substrate bias has little effect on the potential in the buried channel due to the capacitor voltage divider effect, and the gate voltages can be set independently of the substrate bias.

In addition, a thick CCD reduces fringing [17]. In thinned CCD's fringing arises due to multiple reflections at long wavelengths when the absorption length of the incident light is greater than the CCD thickness. Fringing as well as the loss of QE limits the usefulness of scientific CCD's at long wavelengths.

There are several drawbacks to a thick CCD, however. Charged-particle events from cosmic rays and terrestrial radiation sources will affect more pixels in a thick CCD [18]. Also, a larger volume for near-infrared response implies more volume for dark current generation and care must be taken during processing to minimize dark current. In addition, reduction of surface current due to interface states is not as straightforward as in a thinned CCD with no substrate bias, although as shown later surface dark current suppression can be done satisfactorily at cryogenic temperatures.

Also, in low-f number optical systems where the light is incident at large angles from the normal, there will be depth of focus issues for long-wavelength light absorbed at significant depths, although the large refractive index of silicon helps in this regard by "straightening" the light. At the short wavelength end, the photogenerated holes must traverse nearly the entire thickness of the CCD, and spatial resolution is a concern. These topics are discussed in more

detail in the remainder of the paper. In the next section the fabrication technology is described, followed by discussion of transistor behavior of buried channel MOS devices fabricated on high-resistivity silicon.

As a practical matter it is not convenient to make an explicit electrical connection to the back side of the wafer as shown in Figure 1. Doing so would complicate the use of insulating anti-reflecting coatings, for example. Instead, in the actual implementation of the CCD the contact is made on the front side of the CCD. An implanted n^+ ring surrounds a series of floating p^+ guard rings [19], [20], [21] that drop the potential from the undepleted n region, where the n^+ ring is located, to a grounded p^+ guard ring that surrounds the CCD. Photo-generated electrons are drained to the n^+ contact via a backside ohmic contact that will be described later.

III. CCD Fabrication and Back-Illumination Technology

The CCD's discussed in this work were fabricated at the Lawrence Berkeley National Laboratory Microsystems Laboratory [3]. The starting material was 100 mm diameter, (100), high-resistivity, n-type silicon.

The gate insulator consists of 500 Å of thermally grown SiO_2 and 500 Å of low-pressure chemical vapor deposited (LPCVD) Si_3N_4. The triple polysilicon gate structures are plasma etched in Cl_2/HBr for high selectivity to the underlying Si_3N_4 layer. Single-level Al-Si is used for metallization. In-situ doped (phosphorus) polysilicon is used for extrinsic gettering [6], and this layer is deposited on the back side of the wafer early in the process and capped with Si_3N_4 to eliminate oxidation of the layer and possible autodoping during subsequent processing. A notch implant [22] is included in the process and is used in the serial register to confine small-signal charge packets to a 3 μm wide channel in the serial register, which is wider than the vertical channel to accommodate binning.

Figure 3 shows an example of a 100 mm diameter wafer fabricated at LBNL. The large devices in the center of the wafer are 2048 × 2048, 15 μm pixel, frame transfer CCD's with two amplifiers and optional frame store operation. The wafer also includes additional 15 and 24 μm pixel CCD's.

Since the structure shown in Figure 1 is essentially a CCD merged with a p-i-n diode, we require a backside ohmic contact in order to apply the substrate bias needed to fully deplete the wafer thickness. This ohmic contact layer must be thin to allow for short-wavelength light detection. In Figure 2 it can be seen that the absorption length is less than 0.1 μm for wavelengths less than about 400 nm, and becomes less than 100 Å at ultraviolet (UV) wavelengths.

Previous back-illumination techniques for conventional scientific CCD's include UV flooding [23] and laser annealing of an ion implanted backside layer [10], [24]. In both cases a built-in field is generated to overcome the native depletion layer at the backside surface for p-type silicon due to positive fixed oxide charge at the silicon-SiO_2 interface [1]. Laser annealing is required since the thinning step is performed on a finished wafer and the annealing temperature of the backside implant is limited to ≈ 475–525°C depending on the metallization used [25].

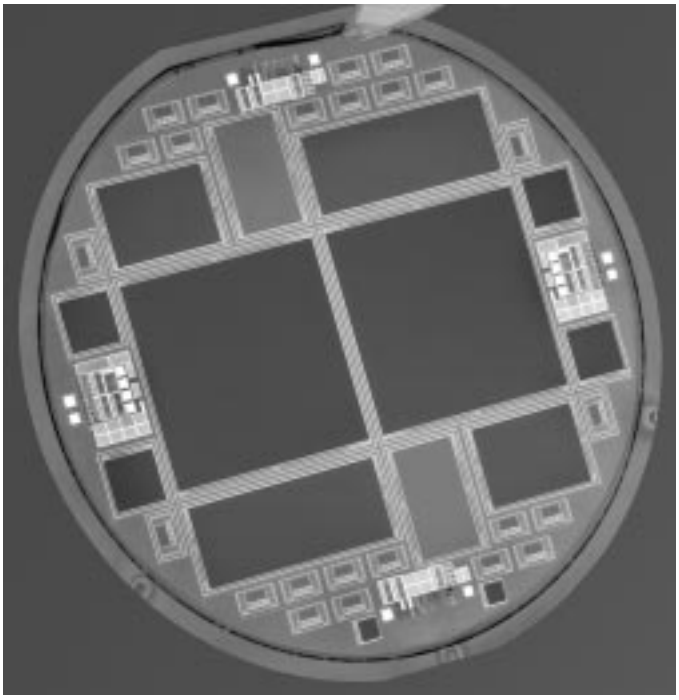


Fig. 3. 100 mm diameter wafer fabricated at LBNL. The two large CCD's in the center of the wafer are 2048 × 2048, 15 μm pixel, frame transfer CCD's.

Since the devices fabricated on high-resistivity silicon can be made relatively thick, it is possible to create the backside layer as a high-temperature step before the Al is deposited. Our technique involves removing the ≈ 1 μm thick n^+ polysilicon gettering layer before the contact mask. The wafers are then sent to a commercial vendor for backside polishing to the final desired thickness. Polishing of the backside surface is required for an optical quality surface, and in our experience this is especially an issue for long-wavelength light.

After the polishing step the backside ohmic contact is formed by depositing a thin layer of in-situ doped (phosphorus) polysilicon [26]. This layer is deposited by LPCVD at 650°C using 1.5% PH_3 in SiH_4 as the source gas. A sacrificial oxide is then sputtered on the back side and the wafers are processed through the contact and metal steps. During these steps the wafers are thinner than standard; we have found that 200 - 300 μm thick, 100 mm diameter wafers can be processed with standard processing equipment. This becomes more challenging as one scales to larger diameter wafers. Modification of some automatic wafer handling equipment was required in order to avoid damaging the backside surface, as well as to minimize particle deposition on the back side. In addition, particle removal via scrubbing is used to reduce the final particle count on the back side of the wafer. If this is not done, uniformly illuminated images (flat fields) taken in the UV can show particle patterns from the various wafer handlers used in the process.

Figure 4 shows a secondary ion mass spectroscopy

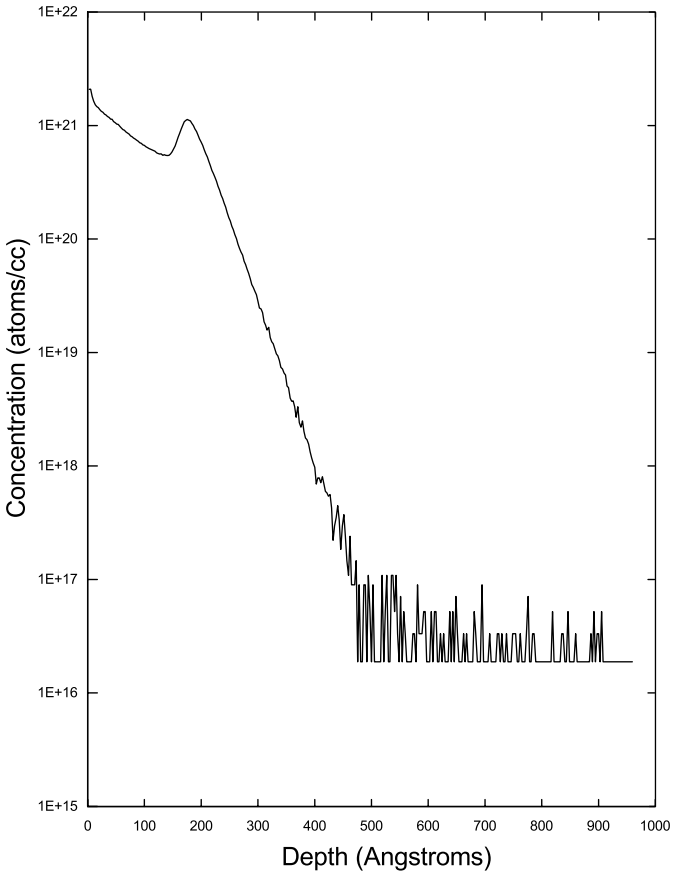


Fig. 4. Secondary ion mass spectroscopy depth profile of the thin back side ohmic contact used in this technology. The layer is fabricated by in-situ doped (phosphorus) polysilicon deposition. The detection limit for phosphorus was 1 $\times 10^{16}$ cm^{-3}.

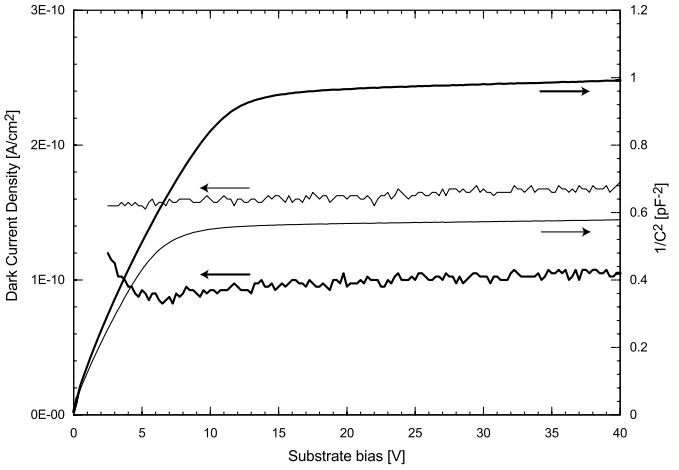


Fig. 5. Inverse square capacitance and reverse leakage current measured at room temperature on 2 mm^2 p-i-n diode test structures from CCD wafers. Data are shown for 200 μm (light) and 275 μm (dark) thick wafers.

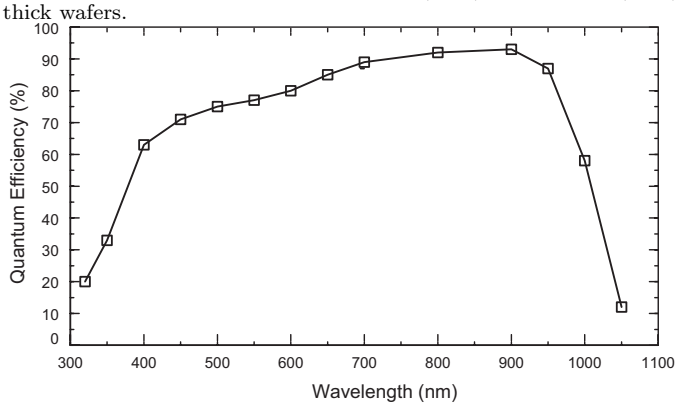


Fig. 6. Quantum efficiency measured on a 1980 $\times$ 800, 15 μm pixel back-illuminated, fully-depleted CCD. The measurement was performed at Lick Observatory and the operating temperature was -130°C. The thickness was $\approx$ 280 μm.

(SIMS) depth profile of the phosphorus concentration for a nominal 200 Å thick backside polysilicon film. The detection limit was 1 $\times 10^{16}$ cm^{-3} and the spatial resolution limit was 65 Å /decade. As can be seen in Figure 4 a very thin layer is possible with this technique. The peak in the phosphorus concentration could be due to phosphorus pile-up at the original polysilicon-silicon interface resulting from perhaps a native oxide layer present at that interface [27]. In general this is not desirable due to the potential for a built-in field that would oppose hole flow for carriers generated in the polysilicon layer, although low collection efficiency is expected there because of low minority carrier lifetime due to Auger recombination.

It will be shown later that it is desirable to operate the CCD over depleted to minimize degradation in spatial resolution. In addition, the fairly large radial variation in resistivity for high-resistivity silicon [28] requires over depleted operation to guarantee the elimination of field-free regions with correspondingly poor spatial resolution. A possible concern is the effect on dark current for over depleted operation. Figure 5 shows measured dark current and inverse square capacitance $1/C^2$ measured on 2 mm^2 p-i-n diode test devices. Results are shown from wafers of thickness $\approx$ 200 and 275 μm. These wafers went through the entire CCD process. The backside polysilicon thickness is $\approx$ 200 Å. The dark current at room temperature is less than 0.2 nA/cm^2, and does not increase significantly for bias voltages above that necessary for full depletion, where the $1/C^2$ curves flatten out. Therefore the gettering process is effective in maintaining low dark current for large depletion depths, and the thin polysilicon deposition step does not degrade the dark current.

After the 400°C sintering step the back side sacrificial oxide is removed and $\approx$ 600 Å of indium tin oxide (ITO) is deposited [26]. The ITO functions as an anti-reflection (AR) coating and improves the conductivity of the back side, where an equipotential is desired. A second AR coating of $\approx$ 1000 Å of SiO_2 is added to form a 2-layer AR coating optimized for near-IR detection [17]. Figure 6 shows measured QE of an $\approx$ 280 μm thick, 1980 $\times$ 800, 15 μm pixel back-illuminated CCD with the two-layer AR coating. The QE exceeds 90% at near-infrared wavelengths, and is still $\approx$ 60% at a wavelength of 1 μm.

IV. Transistor Performance

The CCD's described in this work have conventional floating diffusion amplifiers, and p-channel MOSFETs are used for floating diffusion reset and amplification. The output source follower is buried channel to minimize $1/f$

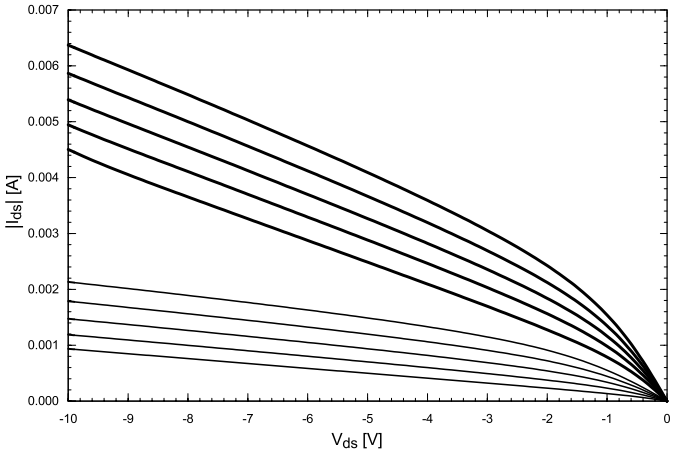


Fig. 7. Room temperature output characteristics of a 51/2 buried channel PMOSFET with 1.5 μm gate to source/drain spacing (lower curves) compared to a self-aligned transistor (upper curves). The substrate bias was 25V. The gate voltage was varied from 7.5 to 3.5V in 1V steps.

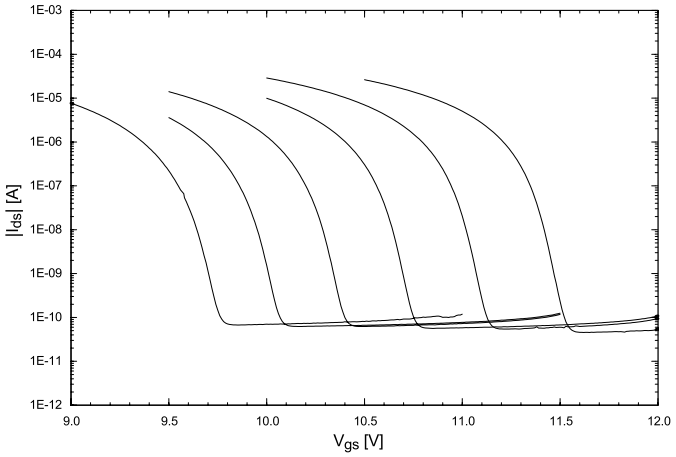


Fig. 8. Measured subthreshold characteristics of a 47/6 buried channel PMOSFET with 1.5 μm gate to source/drain spacing. The substrate bias varied from 25V (rightmost curve) to 75V (leftmost curve) in 10V steps. The temperature was -128°C, and the drain to source voltage was -1V.

noise [29], as is the reset transistor. The transistors are fabricated directly in the high-resistivity substrate. Several examples of active devices fabricated directly on high-resistivity silicon for high-energy physics applications have been reported [30], [31], [32], as well as early work on MOS transistors fabricated on high-resistivity silicon [33], [34].

The use of extremely low substrate doping in an MOS transistor leads to desirable features such as small bulk-junction capacitance and body effect, as well as undesirable features such as punchthrough and drain-induced barrier lowering. The latter two effects can be reduced somewhat by the application of the substrate bias used to fully deplete the substrate [3], [31]. In addition, the heavily doped source and drain regions can be offset from the gate to improve punchthrough characteristics [35], [36] as well as minimize overlap capacitance [7].

The effectiveness of a 1.5 μm source-drain to gate offset in improving the transistor characteristics is shown in Figure 7. Output characteristics of transistors with 2 μm channel length are shown. The self-aligned transistor has a significant threshold voltage change as well as higher output conductance when compared to the device with the 1.5 μm gap between the gate edge and heavily-doped source and drain.

The small body effect realized for these transistors is demonstrated in Figure 8, which shows subthreshold characteristics measured on a 47/6 MOSFET with 1.5 μm gate to source/drain spacing at a temperature of -128°C for substrate bias voltages ranging from 25V to 75V. Over this 50V range in substrate bias the threshold voltage of the transistor is changed by only $\approx$ 1.8V, which can easily be accommodated in the CCD biasing. The data of Figure 8 were measured on a CCD with access to the gate electrode through the reset transistor. The CCD was mounted in a commercially available cryogenic dewar. The high off-state leakage current is an artifact of the measurement, and is due to leakage current in the dewar wiring. This device had a boron channel implant dose of 1.3×10^{12} cm^{-2}. The measured subthreshold slope at -128°C is 50–56 mV/decade.

Hence the transistor characteristics are adequate for scientific CCD applications even for devices fabricated on 10,000–12,000 Ω-cm silicon. In the next section we present data on CCD performance.

V. CCD performance

Figure 9 shows a far red/near infrared image of the Dumbbell Nebula M27 taken at the National Optical Astronomy Observatory WIYN 3.5–meter telescope [37] with a back-illuminated 2048 $\times$ 2048, 15 μm pixel CCD of the type shown in Figure 3. This is a false color image taken from exposures with three different filters; a narrow-band filter at the H-α line (6560 Å, blue in the image), a narrow-band filter at the [SIII] line (9532 Å, green in the image), and an intermediate band filter that detects HeII emission (1.0124 μm, red in the image).

For comparison a visible light image taken at the European Southern Observatory 8.2–meter Very Large Telescope (VLT) is shown in Figure 10 [38]. This image was taken with a commercially available, back-illuminated 2048 $\times$ 2048, 24 μm pixel CCD. The image is also generated from three filters, although in this case the filters are all in the visible range; a narrow-band filter centered at the [OIII] emission line (5010 Å, green in the image), a narrow-band filter centered at the H-α emission line (6560 Å, red in the image), and a broad band filter centered at 4290 Å (blue in the image).

The H-α detail is shown nicely in both images. The main difference in the images is the detection of background stars in the 1.0124 μm exposure, which are not seen in the image of Figure 10 due to absorption of the visible wavelengths of the background light in the dust and gas in the vicinity of the nebula. Imaging at $\approx$ 1 μm with high quantum efficiency and negligible fringing is a unique feature of a fully-depleted, thick CCD.

Figures 11 and 12 show charge transfer efficiency (CTE) and noise results. Charge transfer efficiency was measured

Fig. 9. Far red/near infrared image of M27 (Dumbbell Nebula) taken with a fully-depleted, back-illuminated 2048 × 2048, 15 μm pixel, high-resistivity CCD. The image was generated from exposures taken at three wavelengths (see text) at the National Optical Astronomy Observatory WIYN 3.5 meter telescope [37].

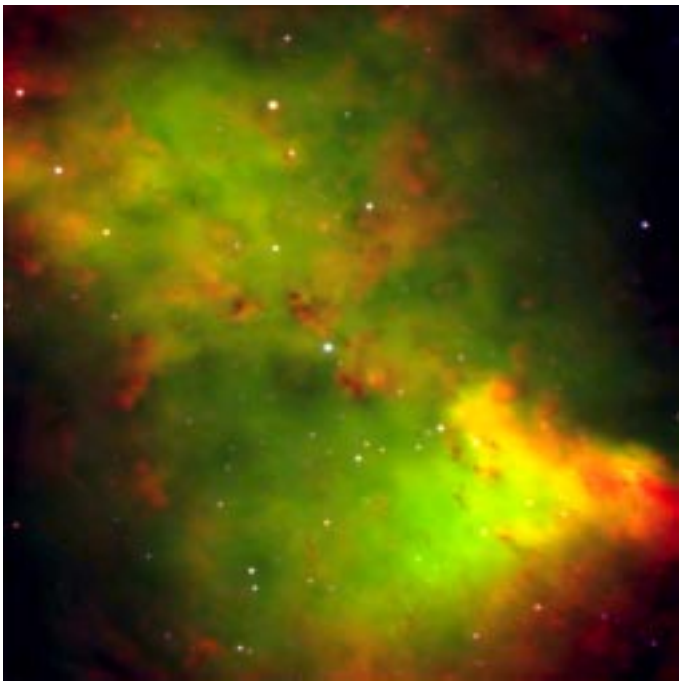


Fig. 10. Visible light image of M27 (Dumbbell Nebula) taken with a commercially available, back-illuminated 2048 × 2048, 24 μm pixel CCD. The image was generated from exposures taken at three wavelengths (see text) at the European Southern Observatory 8.2- meter Very Large Telescope (VLT) [38].

with an ^{55}Fe source [1] on a front-illuminated, 1478 × 4784, 10.5 μm pixel CCD. The CTE at −130°C exceeds 0.999995, and that is typical for devices fabricated on high-resistivity silicon at LBNL. The data were truncated at ≈ 3700 rows due to decreasing x-ray counts resulting from the finite size of the x-ray source. Nonetheless, 3700 rows corresponds to a transfer length of ≈ 4 cm.

The read noise was previously reported to be 4–6 electrons [4], and has been improved to as low as ≈ 2 electrons by reducing the parasitic capacitance at the floating diffusion, as seen in Figure 12. Minimization of the area of the aluminum trace from the floating diffusion to the gate of the output 47/6 MOSFET accounts for most of the improvement noted in Figure 12. Even lower noise has been reported with the use of a buried contact technology to minimize the interconnect capacitance [10].

Dark currents of a few electrons per pixel per hour have been achieved at low temperatures. The importance of gettering to achieve low dark current was previously described. Surface dark current arising from interface states is also an important issue. In typical scientific CCD's the surface dark current is reduced by operating the surface of the buried channel in inversion at least part of the clock cycle [39], [40], [41].

Supply of inversion layer carriers from the channel stop is not straightforward when relatively large substrate bias voltages are applied, as in the case of the CCD's considered in this work. This is a drawback to the use of a substrate bias to fully deplete the CCD. Nonetheless, one can take advantage of the temperature dependence of the time constant for detrapping of charges trapped in interface states [42]. At the low operating temperatures considered here, the time constants are on the order of hours. Figure 13 shows experimental data taken at −150°C on a back-illuminated, 2048 × 2048 CCD. The CCD was exposed to a light level sufficient to bloom charge to the interface states. This charge gradually detraps during subsequent dark frames, resulting in a residual image. After 14 hours the CCD then goes through an "erase" cycle that consists of lowering the substrate bias to zero volts and increasing the positive vertical clock levels to a value sufficient to invert the surface with electrons from the channel stops. After the erase cycle the CCD is operated with the normal substrate bias voltage and more dark frames are taken. The erase cycle fills the interface states with electrons, and as shown in Figure 13 dark currents on the order of a few electrons per pixel per hour are then achieved at the cryogenic operating temperatures of interest for the astronomy application.

VI. Spatial Resolution

A concern for the fully-depleted, back-illuminated CCD is spatial resolution degradation resulting from lateral spreading via diffusion of the photogenerated charge during the transit from the back side of the device, where short-wavelength light is absorbed, to the CCD potential wells located as far as 300 μm away. We first analyze the charge spreading for the case of a fully-depleted substrate. The charge spreading is described by the point spread function (PSF), which is the impulse response of the optical system [43]. It can be shown that for carriers arriving at the potential wells at the same time that the solution to the continuity equation for the lateral charge spreading is Gaussian [44]. The charge spreading is characterized by

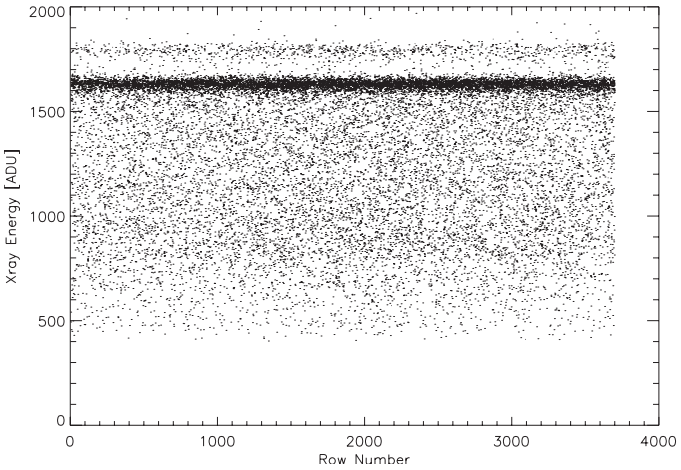


Fig. 11. Vertical charge transfer efficiency measured at −130°C on a 1478 × 4784, 10.5 μm pixel CCD.

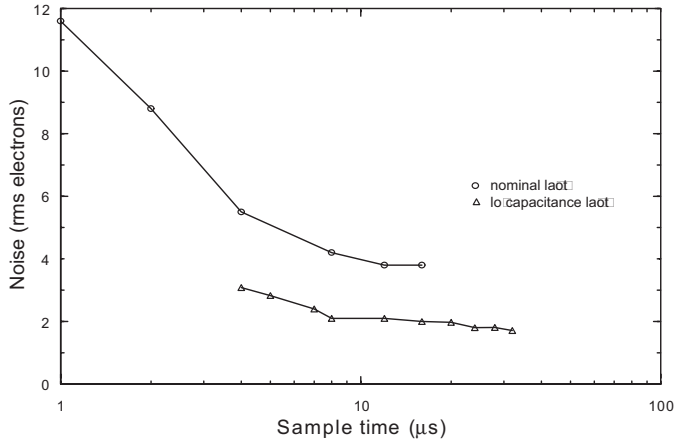


Fig. 12. Noise after double-correlated sampling versus sample time at −130°C comparing 47/6 output transistors with varying size metal interconnect between the floating diffusion and output transistor.

a standard deviation σ given by $\sqrt{2D\,t_{\rm tr}}$ where D is the diffusion coefficient and $t_{\rm tr}$ is the carrier transit time [45]. Assuming the fields are below the velocity saturation limit, the drift velocity of the holes is given by

$$v_{\rm DRIFT} = \frac{dy}{dt} = \mu_p E(y) = \mu_p(E_{\rm max} + \frac{\rho_n}{\epsilon_{\rm Si}} y) \qquad (4)$$

where $E(y)$ is the electric field and μ_p is the hole mobility. The expression for $E(y)$ given above is for the case of a simple p^+–n^-–n^+ structure that is overdepleted. $\rho_n = q\,N_D$ is the volume charge density in the depleted region. $E_{\rm max}$ is the field at the p-n junction and is given by

$$E_{\rm max} = -\left(\frac{V_{\rm appl}}{y_D} + \frac{1}{2}\frac{\rho_n}{\epsilon_{\rm Si}} y_D\right) \qquad (5)$$

where $V_{\rm appl}$ is the voltage drop across the drift region and is assumed to be larger than the depletion voltage, $\rho_n\,{y_D}^2/(2\,\epsilon_{\rm Si})$. The origin is taken at the p-n junction where $E = E_{\rm max}$, and the n^+ region begins at y_D, *i.e.* y_D is the thickness of the depleted region and $E(y_D) = E_D$.

Solving Eq. 4 and making use of the Einstein relation $D/\mu_p = kT/q$ yields

$$\sigma_{od} = \sqrt{2D\,t_{\rm tr}} = \sqrt{2\frac{kT}{q}\frac{\epsilon_{\rm Si}}{\rho_n}\ln\frac{E_{\rm max}}{E_D}} \qquad (6)$$

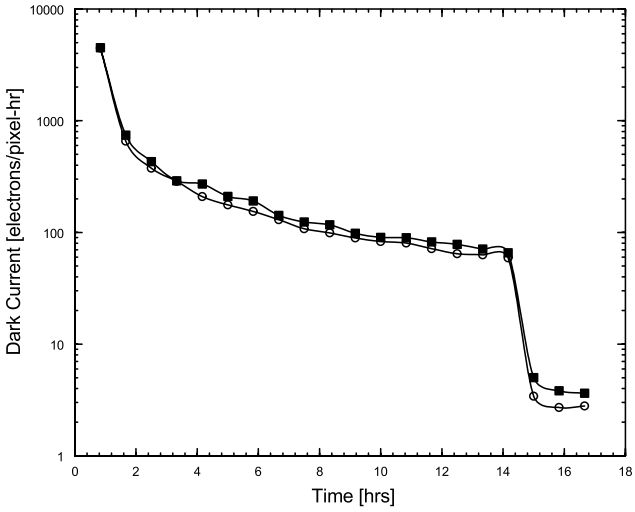


Fig. 13. Dark current versus time measured at −150°C for a back-illuminated, 2048 × 2048 CCD. At time zero the CCD is overexposed to light, resulting in a residual image that detraps with a long time constant at −150°C. After 14 hours the "erase" cycle described in the text is employed to erase the residual image and reduce the surface dark current by trapping electrons in the interface states. The open symbols are for dark current measured near the serial register, and the closed symbols are for measurements far from the serial register.

The subscript indicates that this result is for an overdepleted region. An implicit assumption used in deriving Eq. 6 is that the photons are absorbed at y_D, which is the worst case. At high fields σ_{od} approaches the constant-field result

$$\sigma_{od} \approx \sqrt{2\frac{kT}{q}\frac{{y_D}^2}{V_{\rm appl}}} \qquad (7)$$

which is independent of N_D, directly proportional to y_D, and proportional to $\sqrt{T}$ and $1/\sqrt{V_{\rm appl}}$. While the above derivation is for a simple p^+–n^-–n^+ structure, the results are also applicable to a fully depleted CCD. The field at the p-n junction of an over depleted CCD is given by (see Appendix A)

$$E_J \equiv -\frac{dV}{dy}(y_J) = -\left(\frac{V_{\rm sub} - V_J}{y_N} + \frac{1}{2}\frac{\rho_n}{\epsilon_{\rm Si}} y_N\right) \qquad (8)$$

which is of the same form as Eq. 5. V_J is the potential at the buried channel junction located at y_J, $V_{\rm sub}$ is the substrate bias voltage, and y_N is the thickness of the lightly-doped, fully-depleted region. V_J was given earlier in Eq. 3. From these equations the maximum field in the drift region depends on both applied voltages (V_G and $V_{\rm sub}$) and the channel implant dose $N_A y_J$.

Eqs. 3 and 8 are derived from a one-dimensional analysis. For CCD's on high-resistivity silicon the potentials are strongly two dimensional [8], [12], since a region exists below the buried channel implant where the field is significantly larger than predicted by Eq. 8. As a practical matter the charge spreading in the high-field region is negligible and Eq. 8 can still be used, but V_J is not the potential at the junction but an average potential where the field deviates from Eq. 8.

We next derive the PSF for conventional back-illuminated scientific CCD's that typically have a region of

zero electric field between the back side illumination surface and the CCD potential wells [1], [46]. The modulation transfer function (MTF) was theoretically analyzed for this case by Crowell and Labuda [47], where MTF is the magnitude of the Fourier transform of the PSF [43]. This work was later extended by Seib [48] to include the possibility of multiple reflections as would occur when the absorption depth of the incident light is larger than the thickness of the device. Details are given in Appendix B, where it is shown that for negligible recombination and light absorbed near the back surface such that the absorption depth is small compared to the field-free thickness, the MTF is given by

$$\mathrm{MTF}_{ff} \approx \frac{1}{\cosh(kL_{ff})} \tag{9}$$

where $k = 2\pi f$ where f is the spatial frequency and L_{ff} is the field-free thickness. The PSF is the inverse Fourier transform of the MTF and is then

$$\mathrm{PSF}_{ff} = \frac{1}{2L_{ff}(\cosh(\pi x/2L_{ff}))} \tag{10}$$

where x is the lateral dimension (see Figure 1). The rms standard deviation can be calculated from the Moment Theorem [49] and is given by

$$\sigma^2 = \frac{-F^{(2)}(0)}{4\pi^2 F(0)} + \frac{1}{4\pi^2}\left[\frac{F^{(1)}(0)}{F(0)}\right]^2 \tag{11}$$

where $F^{(n)}(0)$ is the n^{th} derivative of the Fourier transform F evaluated at the origin. Substitution of Eq. 9 with $k = 2\pi f$ into the above yields the simple result

$$\sigma_{ff} = L_{ff} \tag{12}$$

and hence the rms standard deviation for the field-free case is just equal to the field-free thickness. This result was previously given based on the results of Monte Carlo simulations [50]. The above analysis is highly simplified, and is not rigorously valid given the fact that CCD's do not meet the shift invariance requirement for the use of Fourier transforms in the modeling of MTF and PSF [43], [49].

Nonetheless, it is informative to compare the rms standard deviations of charge spreading for the case of an over depleted substrate (Eq. 7) and where the field-free thickness dominates (Eq. 12). Calculations of CCD depletion depth using the equations in Appendix A for a conventional CCD with no applied substrate bias show that the depletion depth is on the order of ≈ 8 μm for a substrate resistivity of 20 Ω-cm at a gate voltage of 10V with a uniform channel doping of 2×10^{16} cm^{-3}. Hence a typical 20 μm thick back-illuminated CCD fabricated on 20 Ω-cm silicon with no substrate bias could have a σ of about 12 μm. This can be improved with further thinning but at the expense of red response and fringing.

In the over depleted case the lateral diffusion can be reduced by lowering the thickness and/or operating temperature, and by increasing the substrate bias. Figure 14

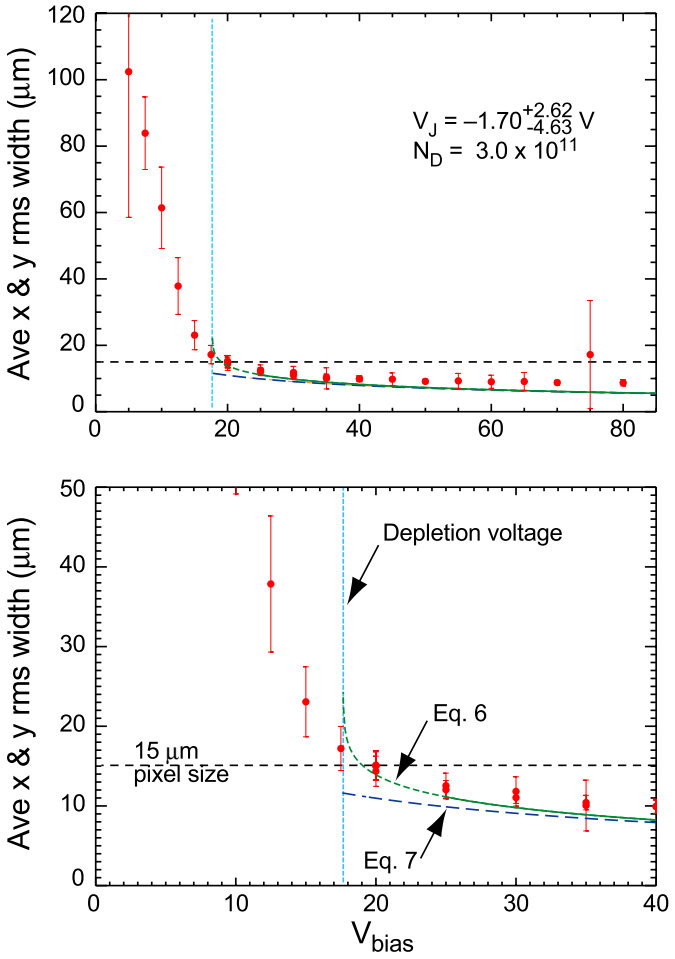


Fig. 14. Measured charge spreading σ using a pinhole mask placed directly on the back side of a back-illuminated CCD fabricated on high-resistivity silicon.

shows experimental data of charge spreading versus substrate bias voltage for an ≈ 300 μm thick CCD at -130°C. The charge spreading was measured by illuminating the CCD through a chrome-on-quartz pinhole mask that was placed directly on the back surface of the CCD. 400 nm light was used in order to maximize the transit distance of the photogenerated holes.

At a typical substrate bias voltage of 40V σ is about 8 - 10 μm, which would be comparable to the theoretical calculation given above for a conventional back-illuminated CCD fabricated on 20 Ω-cm silicon. Therefore, even though the CCD fabricated on high-resistivity silicon is much thicker than its low-resistivity counterpart, the spatial resolution can be comparable and in some cases better. Measurements at the Lick Observatory Hamilton Spectrograph on a 200 μm thick, 2048 × 2048, 15 μm pixel CCD give an overall PSF of ≈ 1.4 pixels full width at half maximum (FWHM), compared to a value of ≈ 2.1 pixels FWHM measured on a thinned, back-illuminated CCD [51].

Figure 14 also includes theoretical curves for the charge spreading. Two parameters, the doping density N_D and potential at the buried channel junction V_J, are required for the theoretical curves shown in Figure 14 (Eqs. 6, 7, 8,

and 3). These are determined from data taken below full depletion where the field-free thickness dominates the σ measurement, and where the field-free thickness varies with N_D and V_J as per simple p-n junction theory, *i.e.* [52]

$$L_{ff} = y_N - \sqrt{\frac{2\epsilon_{\rm Si}}{qN_D}(V_{\rm sub} - V_J)} \qquad (13)$$

A plot of $(y_N - L_{ff})^2$ versus $V_{\rm sub}$ should yield a straight line from which N_D and V_J can be determined.

VII. Summary

Fully-depleted CCD's fabricated on high-resistivity silicon have been shown to have improved characteristics at near-infrared wavelengths when compared to conventional scientific CCD's. Physical operating principles of the fully-depleted CCD have been presented along with technology issues and performance results. Trade-offs in terms of QE and spatial resolution as determined by device thickness and operating temperature can be analyzed based on the results given in this work and optimized for a given application.

VIII. Acknowledgements

The authors gratefully acknowledge Kirk Gilmore, Armin Karcher, and Bill Kolbe for CCD measurements, Guobin Wang for CCD fabrication, Bill Brown for CCD packaging, John Bercovitz for wafer handling equipment modification, Philippe Eberhard for insight into the field-free MTF problem, Nadine Wang for ITO process development, Bill Moses for photodiode QE measurements, Chris Bebek and Michael Levi for overall management, and Arjun Dey and Debra Fischer for their efforts in fielding these CCD's at astronomical telescopes. This work was supported by DOE contract No. DE-AC03-76SF00098 and the National Science Foundation ATI program.

Appendix A: Derivation of potentials and fields for an overdepleted CCD

Figure 15 shows the cross-section of the CCD. The origin is taken at the silicon-SiO_2 interface. The gate insulator thickness is d, the junction depth is at y_J, and the thickness of the substrate is $y_J + y_N$.

The solutions to Poisson's equation subject to the boundary conditions $V(-d) = V_G - V_{FB}$, $V(y_J + y_N) = V_{\rm sub}$, and continuity of electric field and potential at y =0 and y_J are [54]

$$V(y) = V_G - V_{FB} - E_{\rm SiO_2}(y + d) \qquad -d < y < 0 \quad (A1)$$

$$V(y) = V_{\rm min} + \frac{qN_A}{2\epsilon_{\rm Si}}(y - y_P)^2 \qquad 0 < y < y_J \qquad (A2)$$

$$V(y) = V_J - \frac{qN_D}{2\epsilon_{\rm Si}}(y - y_J)^2 - E_J(y - y_J) \qquad y_J < y < (y_J + y_N) \qquad (A3)$$

where $V_J \equiv V(y_J)$, $V_{\rm min} \equiv V(y_P)$, *i.e.*$y_P$ is the location of the potential minimum, and the electric fields are defined by

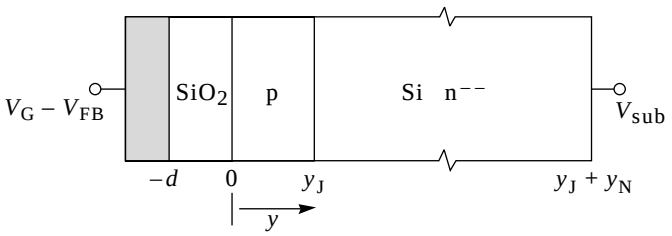


Fig. 15. CCD cross section.

$$E_{\rm SiO_2} \equiv -\frac{dV}{dy}(0^-) \qquad (A4)$$

$$E_J \equiv -\frac{dV}{dy}(y_J) = -\left(\frac{V_{\rm sub} - V_J}{y_N} + \frac{1}{2}\frac{qN_D}{\epsilon_{\rm Si}}y_N\right) \qquad (A5)$$

where the boundary condition $V(y_J + y_N) = V_{sub}$ was used to determine E_J. In terms of terminal voltages E_J is

$$E_J = \frac{V_G - V_{FB} - {V_{\rm SiO_2}}' - {V_J}' - V_{\rm sub}}{y_J + y_N + (\epsilon_{\rm Si}/\epsilon_{\rm SiO_2})\,d} \qquad (A6)$$

where

$${V_{\rm SiO_2}}' \equiv \frac{qN_A}{2\epsilon_{\rm Si}}{y_J}^2\left(1 + \frac{2\epsilon_{\rm Si}d}{\epsilon_{\rm SiO_2}y_J}\right) \qquad (A7)$$

$${V_J}' \equiv \frac{qN_D}{2\epsilon_{\rm Si}}{y_N}^2 \qquad (A8)$$

For the CCD's considered here, $y_N \gg y_J + (\epsilon_{\rm Si}/\epsilon_{\rm SiO_2})\,d$, and Eq. 3 results from Eqs. A5 and A6.

Appendix B: Derivation of PSF for a back-illuminated CCD with a field-free region

A back-illuminated photodiode array consisting of p^+ diodes on n-type silicon, with field-free thickness L_{ff} and total thickness (field-free and depleted depth) L_b was considered in the Crowell and Labuda analysis [47]. Surface and bulk recombination are characterized by surface recombination velocity S and minority carrier lifetime τ. $L_o = \sqrt{D\tau}$ is the diffusion length.

The continuity equation was solved with electron-hole pair generation due to a sinusoidal light source yielding a generation term of

$$G(x, y) = \frac{N_0}{2}\alpha(1 - R)(1 + \cos(kx))\exp(-\alpha y) \qquad (14)$$

where N_0 is the peak photon flux, $k = 2\pi f$ where f is the spatial frequency, and R is the wavelength-dependent reflectivity, which can be determined from optical calculations [17].

The total hole flux $J_p(x)$ consisting of the hole diffusion current entering the depletion region plus the number of holes per unit time and area that are optically generated in the depletion region is given as

$$J_p(x) = (N_0/2)(\eta_0 + \eta_k\cos(kx)) \qquad (15)$$

where

$$\eta_k = \frac{1}{(1-R)}\left[\frac{\alpha L_k}{\alpha^2 {L_k}^2 - 1} \times \gamma - \exp(-\alpha L_b)\right] \quad (16)$$

$$\eta_o = \eta_k \mid_{k=0} \quad (17)$$

$$\begin{aligned}\gamma &= \frac{2(\alpha L_k + SL_k/D) - (\beta_+ - \beta_-)\exp(-\alpha L_{ff})}{\beta_+ + \beta_-} \\ &- (\alpha L_k)^{-1}\exp(-\alpha L_{ff})\end{aligned} \quad (18)$$

$$\beta_\pm = (1 \pm SL_k/D)\exp \pm (L_{ff}/L_k) \quad (19)$$

$$1/{L_k}^2(k) = (1/{L_o}^2) + k^2 \quad (20)$$

Note that η_o models the QE in the presence of surface and bulk recombination for the case of a field-free region at the back surface. A further refinement to the basic quantum efficiency model including an electric field at the back surface was given by Blouke *et al* [46].

In order to simplify the above, we first neglect bulk recombination. This results in $1/L_k(k) \approx k$ with β now given by

$$\beta_\pm \approx (1 \pm S/(Dk))\exp \pm (kL_{ff}) \quad (21)$$

We further assume that the absorption length is small compared to L_{ff}, so that αL_{ff} and αL_b are large. Hence the exponential terms in Eqs. 18 and 16 are neglected, and γ becomes

$$\gamma \approx \frac{2\alpha}{k(\beta_+ + \beta_-)} + \frac{S}{Dk(\beta_+ + \beta_-)} \quad (22)$$

and substitution into Eq. 16 yields

$$\frac{\eta_k}{(1-R)} \approx \frac{2}{\beta_+ + \beta_-} + \frac{S}{\alpha D(\beta_+ + \beta_-)} \quad (23)$$

The MTF neglecting surface recombination is then

$$\begin{aligned}\mathrm{MTF}_{ff} &= \frac{\eta_k}{\eta_o} \\ &\approx \frac{1}{\cosh(kL_{ff})}\end{aligned} \quad (24)$$

This result can be derived from Barbe's Eq. 83 [53], given below, for the case of negligible recombination.

$$\mathrm{MTF}_{ff} \approx \frac{\cosh(L_{ff}/L_o)}{\cosh(L_{ff}/L_k)} \quad (25)$$

References

[1] J.R. Janesick, "*Scientific charge-coupled devices*", SPIE Press, 2001.

[2] S. Perlmutter *et al.*, "Discovery of a supernova explosion at half the age of the Universe," *Nature*, vol. 391, pp. 51-54, Jan. 1998.

[3] S.E. Holland *et al.*, "A 200 × 200 CCD image sensor fabricated on high-resistivity silicon," in *IEDM Technical Digest*, pp. 911-914, 1996.

[4] R.J. Stover *et al.*, "Characterization of a fully-depleted CCD on high-resistivity silicon," in *Proceedings of SPIE*, vol. 3019, pp. 183-188, 1997.

[5] C.H. Sequin, F.J. Morris, T.A. Shankoff, M.F. Tompsett, and E.J. Zimany, Jr., "Charge-coupled area image sensor using three levels of polysilicon," *IEEE Trans. Elec. Dev.*, vol. 21, no. 11, pp. 712-720, Nov. 1974.

[6] S. Holland, "Fabrication of detectors and transistors on high-resistivity silicon," *Nuclear Instrum. Methods in Physics Research A*, vol. 275, pp. 537-541, March 1989.

[7] B.E. Burke, R.W. Mountain, D.C. Harrison, M.W. Bautz, J.P. Doty, G.R. Ricker, and P.J. Daniels, "An abuttable CCD imager for visible and x-ray focal plane arrays," *IEEE Trans. on Electron Devices*, vol. 38, no. 5, pp. 1069-1076, May 1991.

[8] B.E. Burke, R.W. Mountain, P.J. Daniels, M.J. Cooper, and V.S. Dolat, "CCD soft x-ray imaging spectrometer for the ASCA satellite," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 1, pp. 375-385, Feb. 1994.

[9] D. Lumb, H. Eggel, R. Lainé, and A. Peacock, "X-ray multimirror mission - an overview," in *Proceedings of SPIE*, vol. 2808, pp. 326-337, 1996.

[10] B.E. Burke, J.A. Gregory, M.W. Bautz, G.Y. Prigozhin, S.E. Kissel, B.B. Kosicki, A.H. Loomis, and D.J. Young, "Soft-X-Ray CCD imagers for AXAF," *IEEE Trans. Elec. Dev.*, vol. 44, no. 10, pp. 1633-1642, Oct. 1997.

[11] P.S. Heyes, P.J. Pool, and R. Holton, "A new generation of scientific CCD sensors," in *Proceedings of SPIE*, vol. 3019, pp. 201-209, 1997.

[12] D.M. McCann, M.C. Peckerar, W. Mend, D.A. Schwartz, R.E. Griffiths, G. Polucci, and M.V. Zombeck, "Area array x-ray sensors," in *Proceedings of SPIE*, vol. 217, pp. 118-128, 1980.

[13] M.C. Peckerar, D.H. McCann, and L. Yu, "X-ray imaging with a charge-coupled device fabricated on a high-resistivity substrate," *Appl. Phys. Lett.*, vol. 39, no. 1, pp. 55-57, July 1981.

[14] K. Rajkanan, R. Singh, and J. Shewchun, "Absorption coefficient of silicon for solar cell applications," *Solid-State Elec.*, vol. 22, pp. 793-795, 1979.

[15] T.S. Moss, "*Optical properties of semiconductors*," Butterworths Scientific Publications, London, 1959.

[16] J.I. Pankove, "*Optical processes in semiconductors*," Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1971.

[17] D.E. Groom *et al.*, "Quantum efficiency of a back-illuminated CCD imager: an optical approach", in *Proceedings of SPIE*, vol. 3649, pp. 80-90, 1999.

[18] D.E. Groom *et al.*, "Radiation events in astronomical CCD images", to be published, *Proceedings of SPIE*.

[19] Y.C. Kao and E.D. Wolley, "High-voltage planar p-n junctions," *Proceedings of the IEEE*, vol. 55, no. 8, pp. 1409 - 1414, August 1967.

[20] M.S Adler, "Theory and breakdown voltage for planar devices with a single field limiting ring," *IEEE Trans. Elec. Dev.*, vol. 24, no. 2, pp. 107-113, February 1977.

[21] V. Boisson, M. Le Helley, and J.P. Chante, "Analytical expression for the potential of guard rings of diodes operating in the punchthrough mode," *IEEE Trans. Elec. Dev.*, vol. 32, no. 4, pp. 838-840, April 1985.

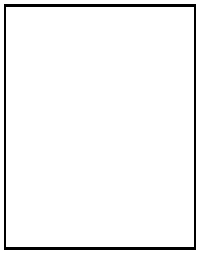
[22] R.A. Bredthauer, J.H. Pinter, J.R. Janesick, and L.B. Robinson, "Notch and large area CCD imagers," in *Proceedings of SPIE*, vol. 1447, pp. 310-315, 1991.

[23] J.R. Janesick, T. Elliot, T. Daud, J. McCarthy, and M.M. Blouke, "Backside charging of the CCD," in *Proceedings of SPIE*, vol. 570, pp. 46-79, 1985.

[24] R.A. Stern, T. Whittemore, M. Winzenread, and M.M. Blouke, "Ultraviolet quantum efficiency and vacuum stability of ion-implanted, laser annealed CCDs," in *Proceedings of SPIE*, vol. 1071, pp. 43-57, 1989.

[25] S. Sedky, A. Witvrouw, H. Bender, and K. Baert, "Experimental determination of the maximum post-process annealing temperature for standard CMOS wafers," *IEEE Trans. Elec. Dev.*, vol. 48, no. 2, pp. 377-385, Feb. 2001.

[26] S.E. Holland, N.W. Wang, and W.W. Moses, "Development of low noise, back-side illuminated silicon photodiode arrays," *IEEE Trans. Nucl. Sci.*, vol. 44, no. 3, pp. 443-447, June 1997.
[27] Personal communication with Ming Hong Yang of Charles Evans and Associates, Sunnyvale, CA.
[28] W. von Ammon and H. Herzer, "The production and availability of high resistivity silicon for detector applications," *Nuclear Instrum. and Methods in Physics Research A*, vol. 226, pp. 94-102, 1984.
[29] R.W. Brodersen and S.P. Emmons, "Noise in buried channel charge-coupled devices," *IEEE Trans. Elec. Dev.*, vol. 23, no. 2, pp. 215-223, Feb. 1976.
[30] V. Radeka *et al*, "Implanted silicon JFET on completely depleted high-resistivity devices," *IEEE Elec. Dev. Lett.*, vol. 10, no. 2, pp. 91-94, Feb. 1989.
[31] G. Vanstraelen, I. Debusschere, C. Claeys, and G. Declerck, "Fully integrated CMOS pixel detector for high energy particles," *Nuclear Instrum. Methods in Physics Research A*, vol. 275, no. 3, pp. 574-579, March 1989.
[32] S. Holland and H. Spieler, "A monolithically integrated detector-preamplifier on high-resistivity silicon," *IEEE Trans. Nucl. Sci.*, vol. 37, no. 2, pp. 463-468, April 1990.
[33] P. Richman, "Complementary MOS field-effect transistors on high-resistivity silicon substrates," *Solid-State Elec.*, vol. 12, pp. 377-383, May 1969.
[34] P. Richman, "Modulation of space-charge-limited current flow in insulated-gate field-effect tetrodes," *IEEE Trans. Elec. Dev.*, vol. 16, no. 9, pp. 759-766, Sept. 1969.
[35] K. Yamaguchi and S. Takahashi, "Submicron gate MOSFET's with channel-doped separate gate structures (SG-MOSFET's)," *IEEE Trans. Elec. Dev.*, vol. 28, no. 7, pp. 888-890, July 1981.
[36] K. Yamaguchi, S. Takahashi, and H. Kodera, "Theoretical study of a channel-doped separate gate Si MOSFET (SG-MOSFET) by two-dimensional computer simulation," *IEEE Trans. Elec. Dev.*, vol. 28, no. 1, pp. 117-120, January 1981.
[37] Image courtesy of Nigel Sharp, Rich Reed, Dave Dryden, Dave Mills, Doug Williams, Charles Corson, Roger Lynds, and Arjun Dey, National Optical Astronomy Observatory, WIYN Observatory, and National Science Foundation.
[38] Image courtesy of the European Southern Observatory.
[39] N. Saks, "A technique for suppressing dark current generated by interface states in buried channel CCD imagers," *IEEE Elec. Dev. Lett.*, vol. 7, no. 7, pp. 131-133, July 1980.
[40] J. Hynecek, "Virtual phase technology: a new approach to fabrication of large-area CCDs," *IEEE Trans. Elec. Dev.*, vol. 28, no. 5, pp. 483-489, May 1981.
[41] J. Janesick, T. Elliott, M. Blouke, and B. Corrie, "Charge-coupled device pinning technologies," in *Proceedings of SPIE*, vol. 1071, pp. 153-169, 1989.
[42] B.E. Burke and S.A. Gajar, "Dynamic suppression of interface-state dark current in buried-channel CCDs," *IEEE Trans. Elec. Dev.*, vol. 38, no. 2, pp. 285-290, February 1991.
[43] J.W. Goodman, "*Introduction to Fourier Optics*," McGraw-Hill, 1969.
[44] D.E. Groom *et al.*, "Point-spread function in depleted and partially depleted CCDs," in *Proc. 4th ESO Workshop on Optical Detectors for Astronomy*, Garching, Germany, 13-16 September 1999.
[45] G.R. Hopkinson, "Analytic modeling of charge diffusion in charge-coupled-device imagers," *Optical Engineering*, vol. 26, no. 8, pp. 766-772, August 1987.
[46] M.M. Blouke, W.A. Delamere, and G. Womack, "A simplified model of the back surface of a charge-coupled device," in *Proceedings of SPIE*, vol. 1447, pp. 142-155, 1991.
[47] M.H. Crowell and E.F. Labuda, "The silicon diode array camera tube," *The Bell System Technical Journal*, vol. 48, pp. 1481-1528, May-June 1969.
[48] D.H. Seib, "Carrier diffusion degradation of modulation transfer function in charge coupled devices," *IEEE Trans. Elec. Dev.*, vol. 21, no. 2, pp. 210-217, March 1974.
[49] J.D. Gaskill, "*Linear systems, Fourier transforms, and optics*," John Wiley and Sons, 1978.
[50] J. Janesick, T. Elliott, S. Collins, T. Daud, D. Campbell, A. Dingizian, and G. Garmire, "CCD advances for X-ray scientific measurements in 1985," in *Proceedings of SPIE*, vol. 597, pp. 364-380, 1985.
[51] Personal communication, Debra Fischer, University of California-Berkeley Astronomy Department.
[52] S.E. Holland *et al.*, "Development of back-illuminated, fully-depleted CCD image sensors for use in astronomy and astrophysics," presented at the 1997 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, Bruges, Belgium, 1997.
[53] D.F. Barbe, "Imaging devices using the charge-coupled concept," *Proceedings of the IEEE*, vol. 63, no. 1, pp. 38-67, Jan. 1975.
[54] S.M. Sze, "*Physics of semiconductor devices*," 2nd Edition, John Wiley and Sons, New York, 1981.



Gerry Murray will process your compuscript, adding "value" to your LaTeX file using a sophisticated text editor. Jeremy Barth will standardize the dimensions you've used, run a spell check, apply SGML tags to structure your document and validate all coding. The editor will "on-screen edit" the file, "size" your artwork and supply you with a laser proof by mail, or by fax, or even e-mail you a postscript version of the file which you can view on your workstation (using OpenWindows, NeXT, or an appropriate postscript viewer). When the editor is finished incorporating your amendments, Tom Bontrager, Mark Pheffer, Dalton Patterson or Chaucer Tran will receive the file and apply their abundant knowledge of typesetting to produce a document of the highest possible quality. A postscript file will be generated, output at 2032dpi on high quality RC paper for final examination by the editor. Christine will incorporate the artwork, the resulting camera-ready-copy will then be shot, the film supplied to the printer and your paper printed in the transaction for all to admire.